Introduction to Electrical Engineering

Assignment #6

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PART I: Gate Basics

Table 1- NAND Gate Truth Table

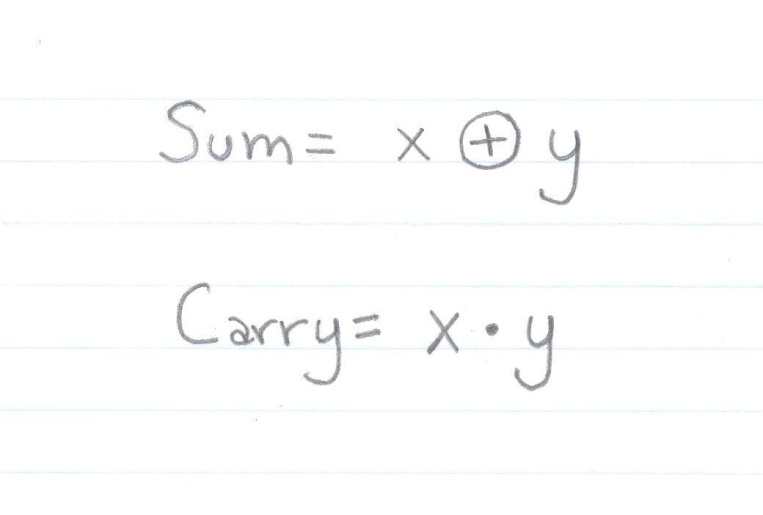
|  |  |  |
| --- | --- | --- |
| A (pin.) | B (pin.) | (AB)’ |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Table 2- NOR Gate Truth Table

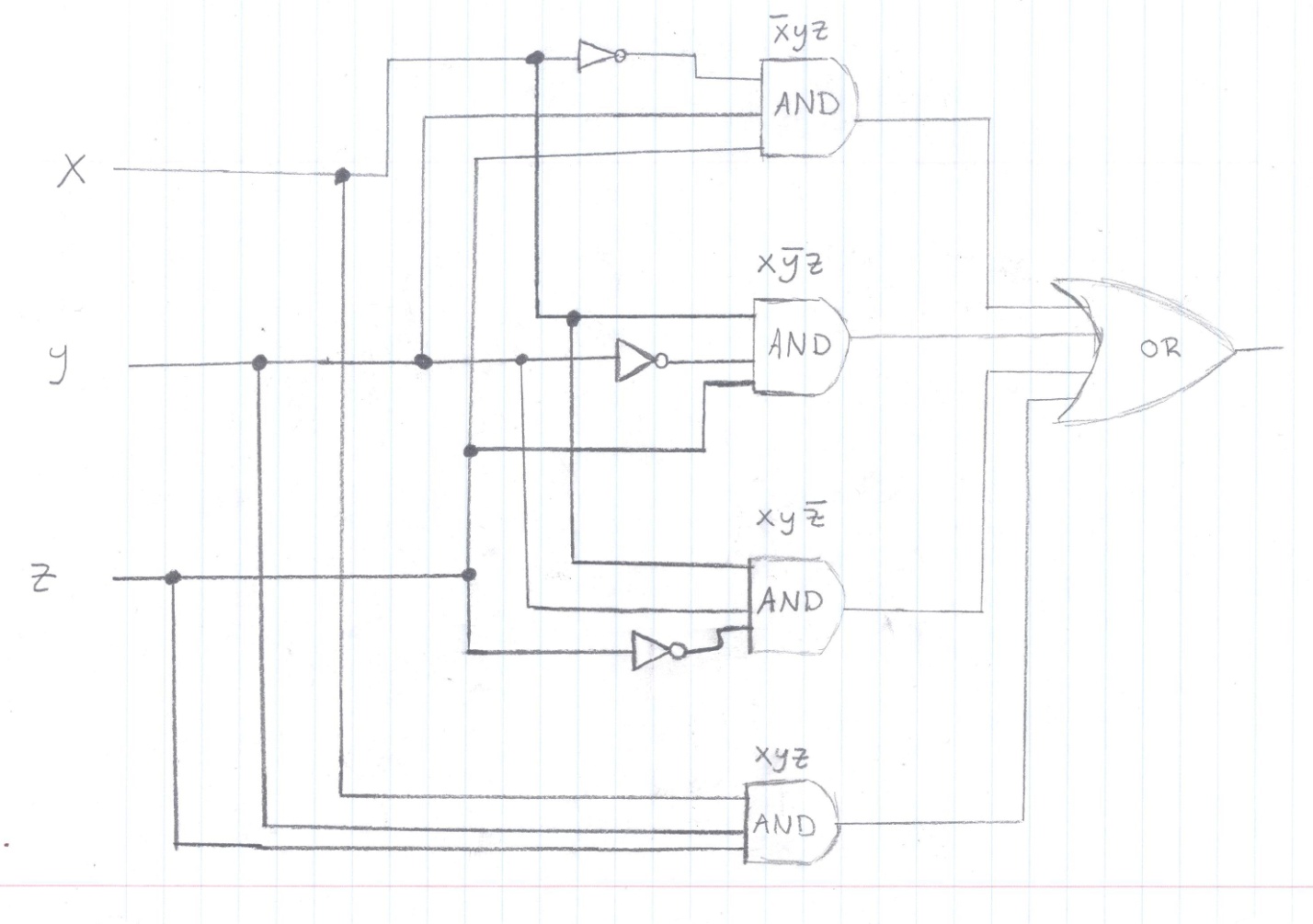
|  |  |  |
| --- | --- | --- |
| A (pin.) | B (pin.) | (A+B)’ |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

Part II: Combinational Circuit

1.



2.



3.

